ABSTRACT OF THE DISCLOSURE

An input circuit includes: a comparator; first and second delay circuits; a selector; an input buffer; and a holding circuit. The comparator compares the leading and/or trailing edges of a data signal, supplied from the input buffer, to an edge of a clock signal on which the data signal is intended to be latched. Based on the results of the comparison, the first and second delay circuits delay the clock signal for respectively predetermined amounts of time. If the data signal is logically high, then the selector selects a delayed clock signal supplied from the first delay circuit. Alternatively, if the data signal is logically low, then the selector selects another delayed clock signal supplied from the second delay circuit. Then, the delayed clock signal, selected by the selector, is latched in the holding circuit. The input circuit with such a configuration prevents skewing from being caused by a difference in length between the transition interval of the data signal from H into L level and that of the data signal from L into H level. As a result, data can be transferred at a much higher speed even if the clock frequency is very high.